

The listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1.-11. (Canceled)

12. (Previously Presented) A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:

forming a MOS transistor on an integrated circuit substrate including an isolation layer and an active region higher than the isolation layer, the MOS transistor having a source region and a drain region on the isolation layer, and a plurality of gates on the active region, the plurality of gates being stacked between the source region and the drain region;

forming a horizontal channel between the source and drain regions, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns, wherein the source and drain regions are vertically formed to cover the sides of the active region in other patterns adjacent to sides of the spaced apart patterns; and

forming a vertical source electrode electrically connected to the source region and a vertical drain electrode electrically connected to the drain region.

13. (Previously Presented) The method of Claim 12, wherein forming the at least two spaced apart horizontal channel region comprises:

forming the active region on the integrated circuit substrate; and

forming at least one epitaxial pattern on the active region and spaced apart from the active region.

14. (Original) The method of Claim 13, wherein forming the at least one epitaxial pattern comprises forming first and second epitaxial patterns, the second epitaxial pattern being on the first epitaxial pattern and spaced apart from the first epitaxial pattern, the method further comprising:

forming a mask pattern on the second epitaxial pattern.

15. (Original) The method of Claim 14, wherein the mask pattern is directly on the second epitaxial pattern.

16. (Previously Presented) The method of Claim 12, wherein forming the source and drain regions comprises forming the vertical source and drain regions, the vertical source region being on a first side of the horizontal channel region and the vertical drain region being on a second side of the horizontal channel region and spaced apart from the vertical source region.

17. (Original) The method of Claim 16, further comprising:
forming a gate pattern on the horizontal channel and between the at least two spaced apart horizontal channel regions; and
forming a gate insulation layer between the gate pattern and the at least two spaced apart horizontal channel regions.

18. (Previously Presented) The method of Claim 17, further comprising:
forming a first insulation pattern between the vertical source and drain electrodes and the integrated circuit substrate and between the gate pattern and the integrated circuit substrate.

19. (Previously Presented) The method of Claim 18, further comprising:
forming a mask pattern on the horizontal channel, wherein the gate pattern extends between an upper channel region of the at least three spaced apart horizontal channel regions and the mask pattern.

20. (Original) The method of Claim 19, further comprising:
forming a second insulation pattern on the horizontal channel and the vertical source and drain regions, wherein the second insulation pattern defines a gate opening on the horizontal channel, wherein the gate pattern is provided in the gate opening and wherein the source and drain electrodes extend through the second insulation pattern and are connected to the vertical source drain regions.

21. (Original) The method of Claim 20, further comprising:
forming a third insulation pattern on the second insulation pattern and the gate pattern,
wherein the source and drain electrodes extended through the third insulation pattern and the
second insulation pattern and are connected to the vertical source and drain regions.

22. (Original) The method of Claim 21, wherein an upper surface of the first
insulation pattern is higher relative to a lower surface of the gate pattern.

23. (Previously Presented) A method of fabricating a transistor comprising:
forming a trench region on an integrated circuit substrate to define an active region;
forming a stacked structure including at least one set of first epitaxial patterns and
second epitaxial patterns on the active region;
forming a first insulation pattern on a floor of the trench;
growing a third epitaxial layer on sidewalls of at least one set of first and second
epitaxial patterns;
forming a second insulation pattern on a surface of the integrated circuit substrate, the
second insulation pattern defining a gate opening that exposes at least a portion of the third
epitaxial layer;
removing the third epitaxial layer in the gate opening to expose the set of at least one
first and second epitaxial patterns;
selectively etching the first epitaxial patterns of the set of at least one first and second
epitaxial patterns to form a horizontal channel region having a plurality of spaced apart
channel layers;
forming a gate oxide layer on a surface of channel layers;
forming a gate pattern on the horizontal channel and in gap regions between the
channel layers and the gate opening; and
forming source and drain electrodes penetrating the second insulation pattern to be
connected to the third epitaxial layer.

24. (Original) The method of Claim 23, wherein forming the trench and a stacked structure further comprises:

alternately stacking sets of first and second epitaxial layers on the integrated circuit substrate; and

patterning the sets of the first and second epitaxial layers and the integrated circuit substrate to form a trench, and sets of the first and second epitaxial patterns.

25. (Original) The method of Claim 23, wherein the first and third epitaxial layers comprise silicon and wherein the second epitaxial layer comprises silicon germanium.

26. (Original) The method of Claim 23, wherein an upper surface of the first insulation pattern is formed lower relative to the first epitaxial layer.

27. (Original) The method of Claim 23, wherein forming the second insulation pattern is preceded by:

forming an etch stop layer conformally on a resultant structure including the third epitaxial layer, wherein forming the gate opening comprises sequentially patterning the second insulation pattern and the etch stop layer and wherein the source and drain electrodes penetrate the etch stop layer to be connected to the third epitaxial layer.

28. (Original) The method of Claim 23, wherein forming the second insulation pattern is preceded by:

implanting impurities in the first and second epitaxial layers to form channel doped layers; and

implanting impurities into the third epitaxial layer to form source and drain regions.

29. (Original) The method of Claim 23, wherein forming the stacking structure of the first and second epitaxial patterns further comprises forming a mask pattern at the upper most layer, and wherein the first and second epitaxial patterns are alternately stacked.

30. (Previously Presented) A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:

forming a horizontal channel between the source and drain regions, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns; and

forming source and drain regions in other patterns at sides of the spaced apart patterns.